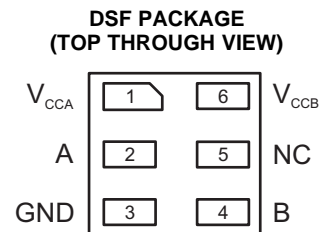
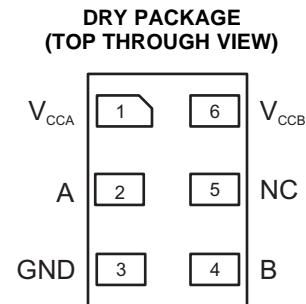
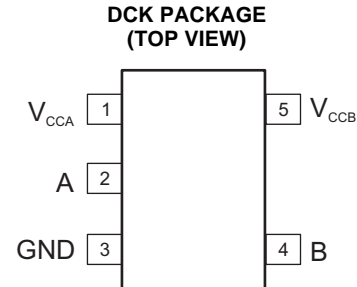


## 1-Bit Unidirectional Voltage-Level Translator

 Check for Samples: [SN74AUP1T34](#)

### FEATURES

- Wide Operating VCC Range of 0.9 V to 3.6 V
- Balanced Propagation Delays:  $t_{PLH} = t_{PHL}$  (1.8 V to 3.3 V Translation Typical)
- Low Static-Power Consumption, 5  $\mu$ A Max ICC
- $\pm 6$  mA Output Drive at 3 V
- $I_{off}$  Supports Partial Power-Down-Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- ESD Protection Exceeds JESD 22
- 5000-V Human-Body Model (A114-A)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II



### DESCRIPTION

The SN74AUP1T34 is a 1-bit non-inverting translator that uses two separate configurable power-supply rails. The A port is designed to track VCCA. VCCA accepts supply voltages from 0.9 V to 3.6 V. The B port is designed to track VCCB. VCCB accepts supply voltages from 0.9 V to 3.6 V. This allows for low-voltage bidirectional translation between 1-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes. The SN74AUP1T34 is also fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	DCK – SOT23	Reel of 3000	SN74AUP1T34DCKR	U2E
	DRY – MicroQFN	Reel of 5000	SN74AUP1T34DRYR	U2
	DSF – MicroQFN	Reel of 5000	SN74AUP1T34DSFR	U2

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### PIN FUNCTIONS

PIN	FUNCTION
VCCA	Input Port DC Power Supply
VCCB	Output Port DC Power Supply
GND	Ground
An	Input Port
Bn	Output Port

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CCA}, V_{CCB}$	Supply voltage range	-0.3	4.0	V
$V_I$	Input voltage range	-0.5	4.6	V
		-0.5	4.6	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state	-0.5	4.6	V
	Voltage range applied to any output in the high or low state	-0.5	4.6	
$I_{IK}$	Input clamp current		-50	mA
$I_{OK}$	Output clamp current		-50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through VCCA or GND		±100	mA
$T_{stg}$	Storage temperature range	-65	150	°C

### RECOMMENDED OPERATING CONDITIONS

		VCCA	VCCB	MIN	MAX	UNIT
$V_{CCA}, V_{CCB}$	Supply voltage			0.9	3.6	V
$V_{IH}$	High-level input voltage	0.9 to 1.95V	0.9 to 1.95V	$0.65 \times V_{CCA}$		V
		2.3 to 2.7V	0.9 to 3.6V	1.6		
		3.0 to 3.6V	0.9 to 3.6V	2		
$V_{IL}$	Low-level input voltage	0.9 V	0.9 to 1.95V		$0.3 \times V_{CCA}$	V
		1 to 1.95V	0.9 to 1.95V		$0.35 \times V_{CCA}$	
		2.3 to 2.7V	0.9 to 3.6V		0.7	
		3.0 to 3.6V	0.9 to 3.6V		0.9	
$\Delta t/\Delta v$	Input transition rise or fall rate	3.0 to 3.6V	0.9 to 3.6V		200	ns/V
$T_A$	Operating free-air temperature			-40	85	°C

**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCCA	VCCB	MIN	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -100 μA	V <sub>I</sub> = V <sub>IH</sub>	0.9 V to 3.6 V	0.9 V to 3.6 V	VCCB - 0.2	V
		I <sub>OH</sub> = -0.25 mA		0.9 V 1V	0.9 V 1V	0.75 x VCCB	
		I <sub>OH</sub> = -1.5 mA		1.2 V	1.2 V	1.0	
		I <sub>OH</sub> = -2 mA		1.65 V	1.65 V	1.32	
		I <sub>OH</sub> = -3 mA		2.3 V	2.3 V	1.9	
		I <sub>OH</sub> = -6 mA		3 V	3 V	2.72	
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	V <sub>I</sub> = V <sub>IL</sub>	0.9 V to 3.6 V	0.9 V to 3.6 V	0.1	V
		I <sub>OL</sub> = 0.25 mA		0.9 V 1V	0.9 V 1V	0.1	
		I <sub>OL</sub> = 1.5 mA		1.2 V	1.2 V	0.3 x VCCB	
		I <sub>OL</sub> = 2 mA		1.65 V	1.65 V	0.31	
		I <sub>OL</sub> = 3 mA		2.3 V	2.3 V	0.31	
		I <sub>OL</sub> = 6 mA		3 V	3 V	0.31	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = VCCA or GND	0.9 V to 3.6 V	0.9 V to 3.6 V		±1	μA
I <sub>off</sub>	A or B port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	0 V	0 V to 3.6 V		±5	μA
			0 V to 3.6 V	0 V		±5	
I <sub>OZ</sub>	A or B port	V <sub>O</sub> = VCCO or GND, V <sub>I</sub> = VCCI or GND, OE = V <sub>IH</sub>	3.6 V	3.6 V		±5	μA
I <sub>CCA</sub>		V <sub>I</sub> = VCCI or GND, IO = 0	0.9 V to 3.6 V	0.9 V to 3.6 V		5	μA
			0.9 V to 3.6 V	VCCA		2	
			0 V	0 V to 3.6 V		1	
			0 V to 3.6 V	0 V		1	
I <sub>CCB</sub>		V <sub>I</sub> = VCCI or GND, IO = 0	0.9 V to 3.6 V	0.9 V to 3.6 V		5	μA
			0.9 V to 3.6 V	VCCA		2	
			0 V	0 V to 3.6 V		1	
			0 V to 3.6 V	0 V		1	
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = VCCI or GND, IO = 0	0.9 V to 3.6 V	0.9 V to 3.6 V		5.2	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.3 V or GND	3.3 V	3.3 V		4	pF
C <sub>io</sub>	A or B port	V <sub>O</sub> = 3.3 V or GND	0 V	3.3 V		7	pF

**AC ELECTRICAL CHARACTERISTICS**

PARAMETER	C <sub>L</sub>	VCCA	VCCB = 0.9 V		VCCB = 1.2 V		VCCB = 1.65 V		VCCB = 2.3 V		VCCB = 3 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
t <sub>PLH</sub> /t <sub>PHL</sub>	5 pF	0.9V	25		18		16.2		16.3		16.8		ns
	5 pF	1.2V		42.5		24.9		23.2		22.6		22.5	
	5 pF	1.65V		40		10.7		8.84		8.08		7.88	
	5 pF	2.3V		41.3		8.02		5.73		4.92		4.2	
	5 pF	3V		42.5		7.61		4.5		3.65		3.39	
t <sub>PLH</sub> /t <sub>PHL</sub>	10 pF	0.9V	28.9		19.8		17.9		18.0		18.5		ns
	10 pF	1.2V		43.22		12.33		9.57		8.81		8.61	
	10 pF	1.65V		40.44		9.21		6.57		5.5		4.73	
	10 pF	2.3V		41.56		8.3		5.54		4.42		4.01	
	10 pF	3V		42.81		7.87		4.55		3.8		3.36	
t <sub>PLH</sub> /t <sub>PHL</sub>	15 pF	0.9V	30.6		21.6		19.6		19.7		20.3		ns
	15 pF	1.2V		43.87		12.98		10.3		9.54		9.34	
	15 pF	1.65V		40.78		9.59		6.95		5.87		5.07	
	15 pF	2.3V		41.79		8.55		5.8		4.68		4.27	
	15 pF	3V		43.09		8.16		4.84		4.09		3.65	
t <sub>PLH</sub> /t <sub>PHL</sub>	30 pF	0.9V	32.1		21.3		18.7		18		18.3		ns
	30 pF	1.2V		45.65		14.76		12.37		11.61		11.41	
	30 pF	1.65V		41.72		10.65		8.01		6.94		5.99	
	30 pF	2.3V		42.44		9.26		6.51		5.39		4.97	
	30 pF	3V		43.69		8.8		5.48		4.72		4.28	

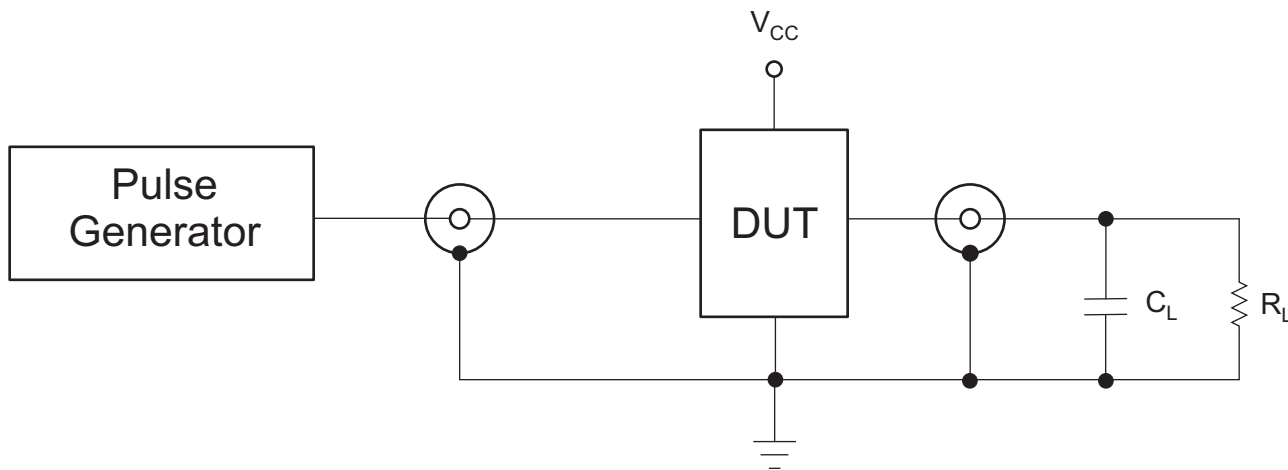
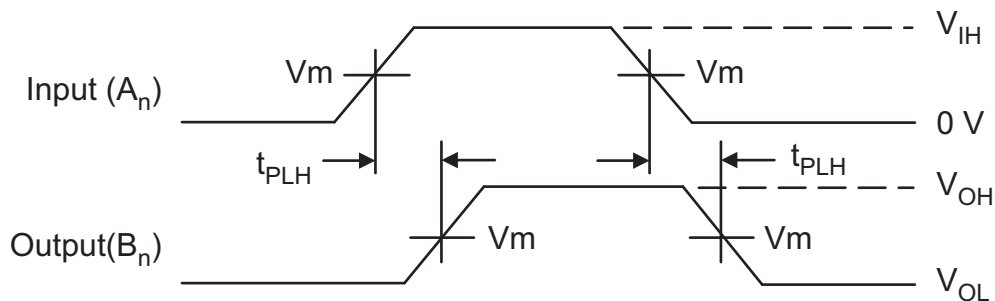


Figure 1. AC (Propagation Delay) Test Circuit

TEST
$t_{PLH}$ , $t_{PHL}$
$C_L = 5 \text{ pF}, 10 \text{ pF}, 15 \text{ pF}, 30 \text{ pF}$ or equivalent (includes probe and jig capacitance)
$R_L = 1 \text{ M}\Omega$ or equivalent
$Z_{OUT}$ of pulse generator = $50 \Omega$



NOTE:  $t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

Figure 2. Waveform 1 - Propagation Delays

## REVISION HISTORY

Changes from Revision A (June 2012) to Revision B	Page
• Removed Feature: Output Enable Feature Allows User to Disable Outputs to Reduce Power Consumption. ....	1

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74AUP1T34DCKR	PREVIEW	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T34DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T34DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**

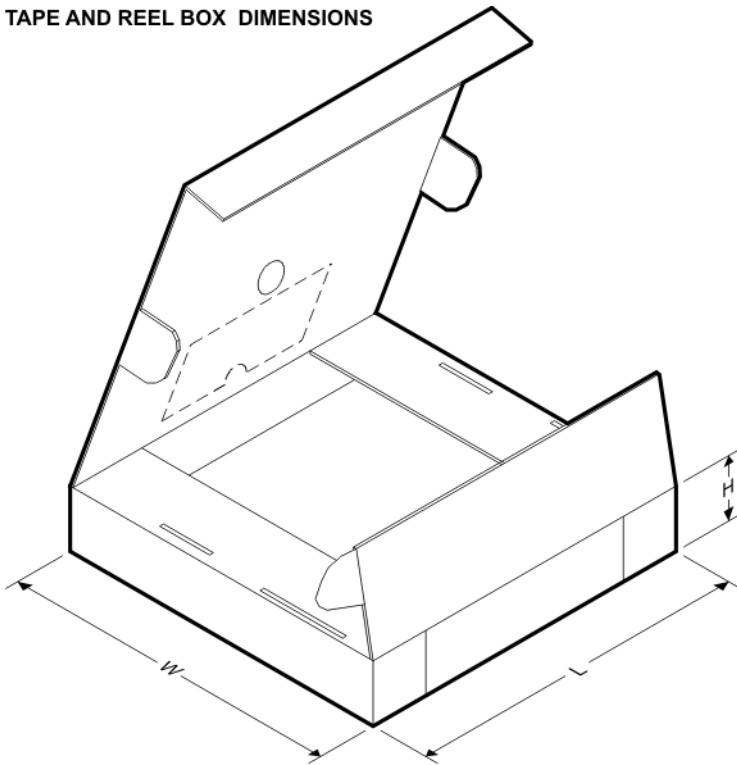

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T34DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1T34DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**



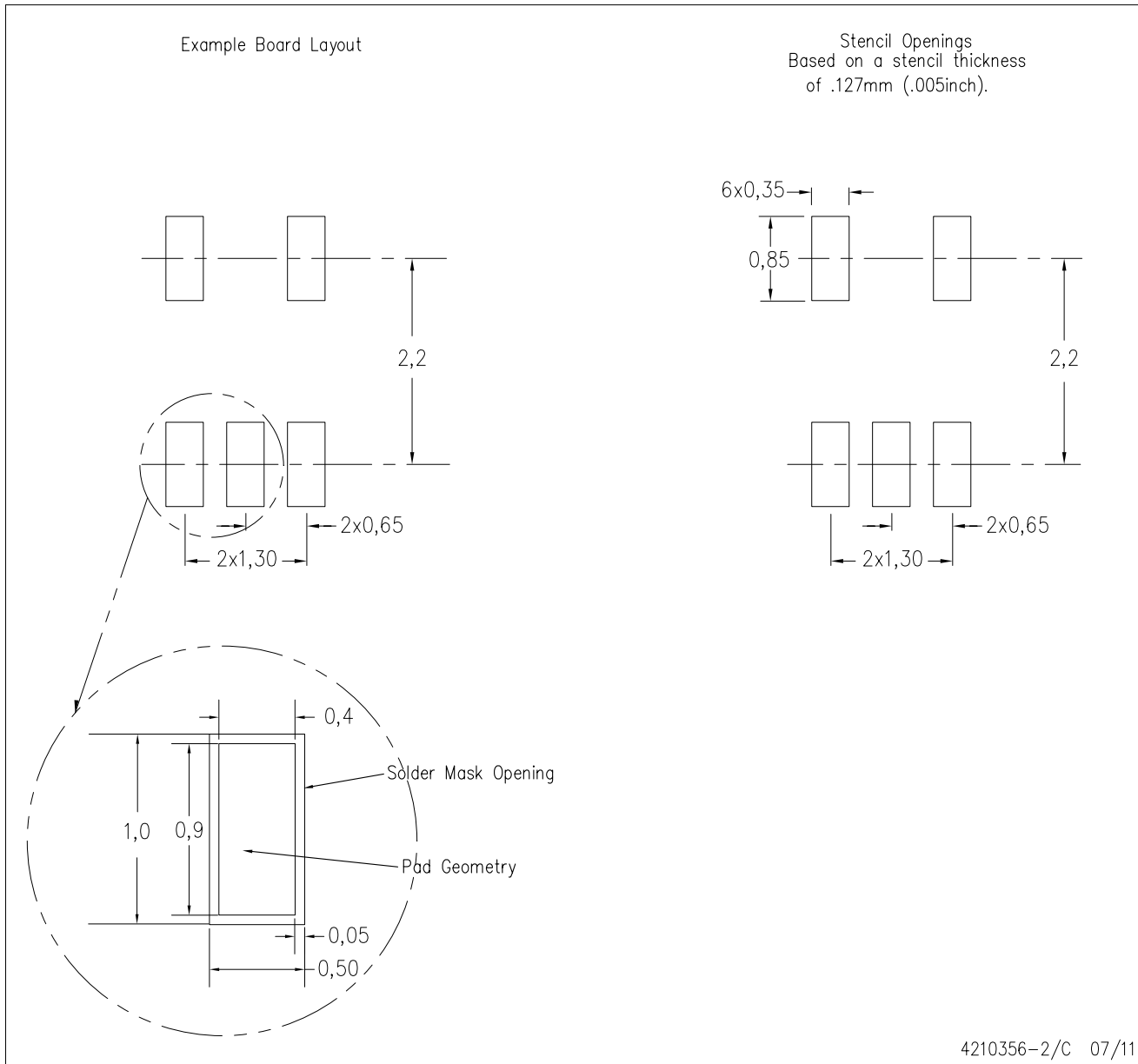
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T34DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74AUP1T34DSFR	SON	DSF	6	5000	180.0	180.0	30.0



DCK (R-PDSO-G5)

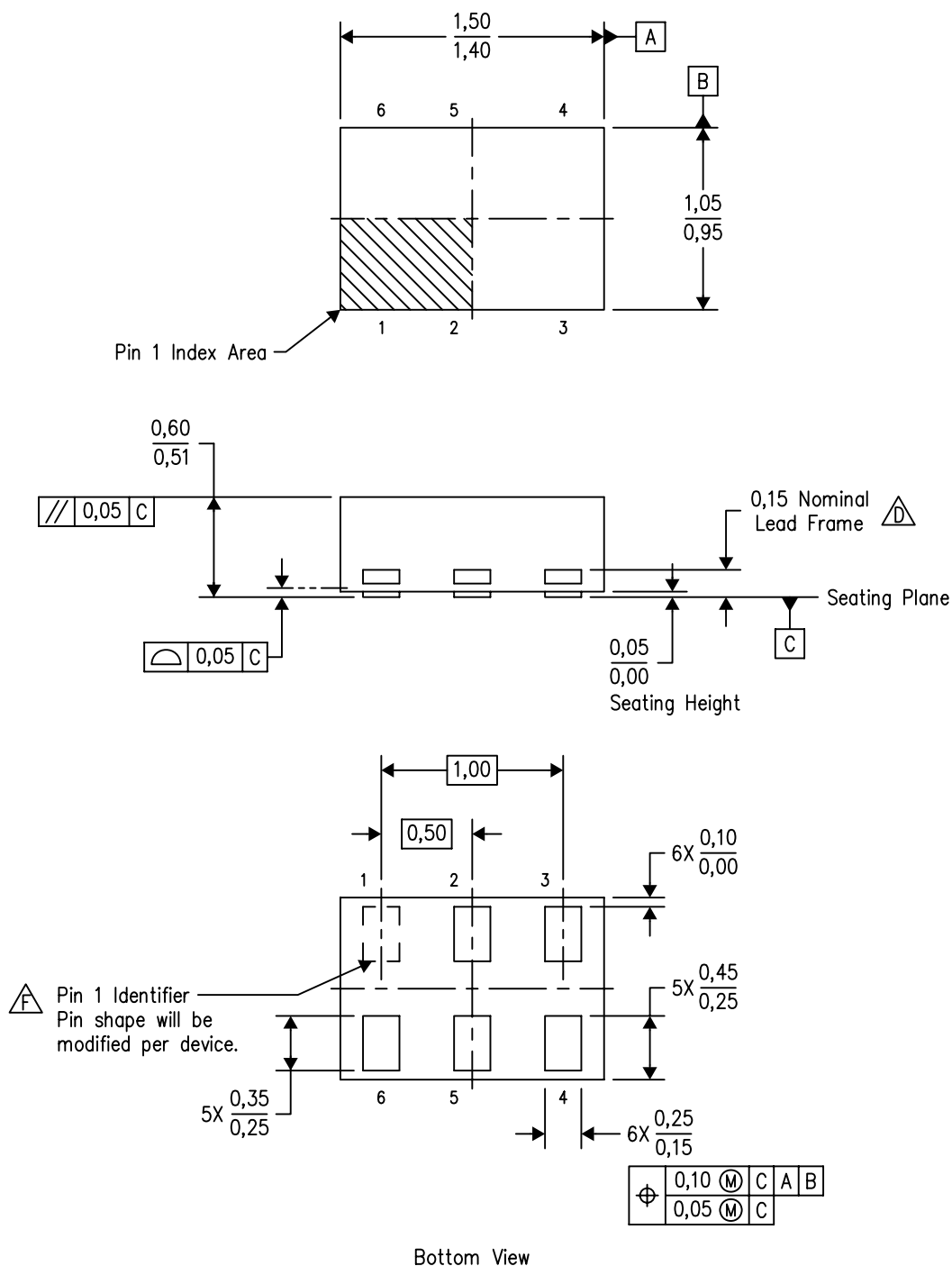
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

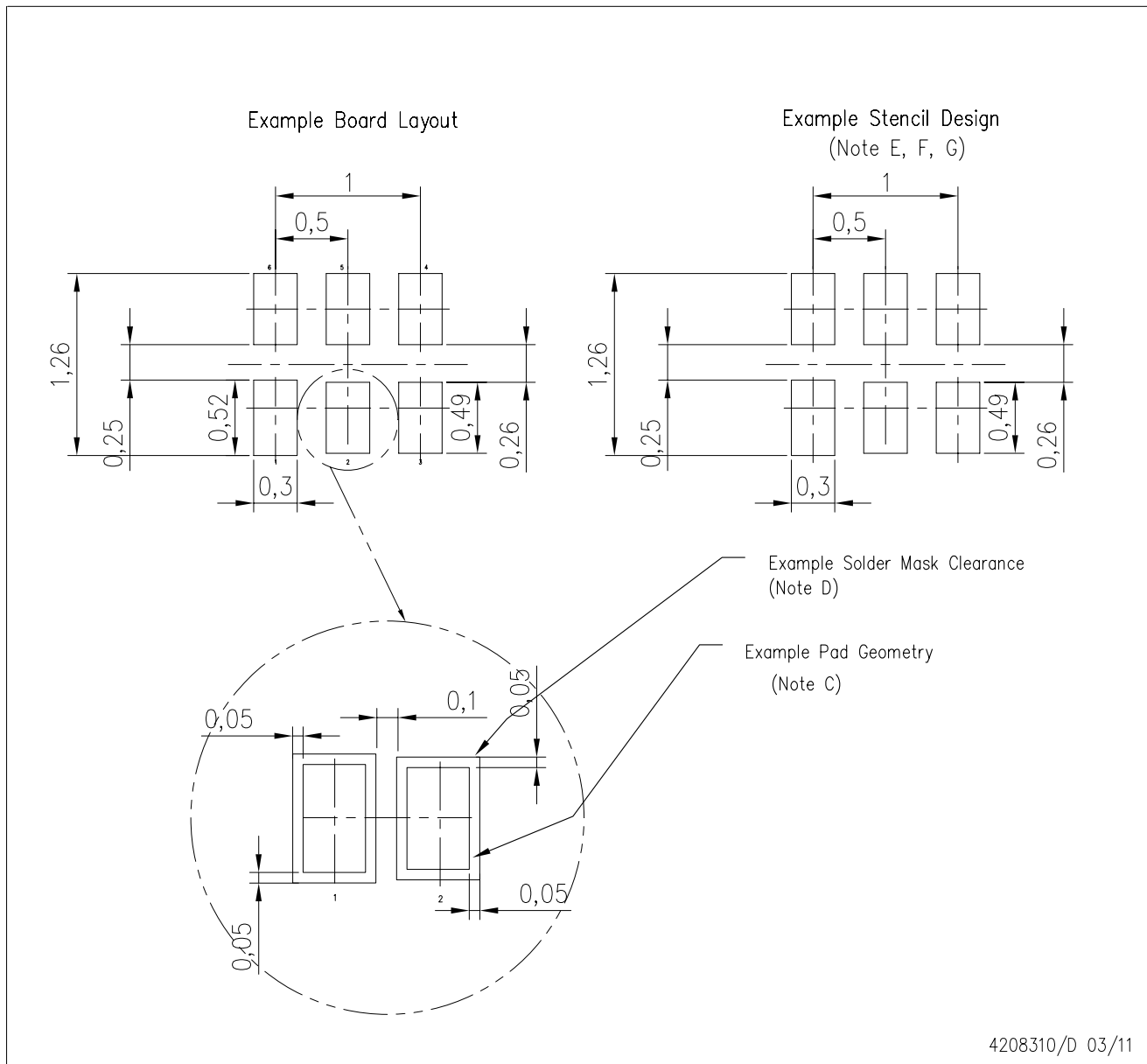


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - $\triangle D$  The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
  - E. This package complies to JEDEC MO-287 variation UFAD.
  - $\triangle F$  See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (S-PUSON-N6)

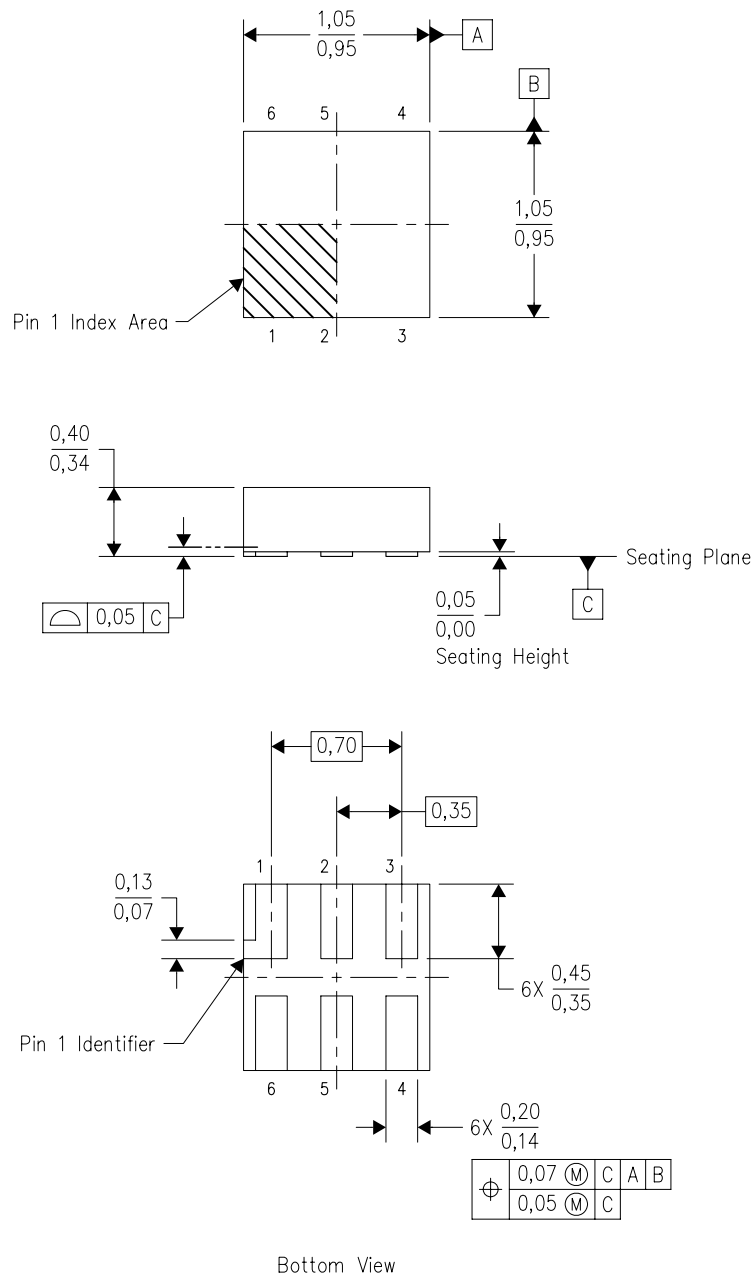
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

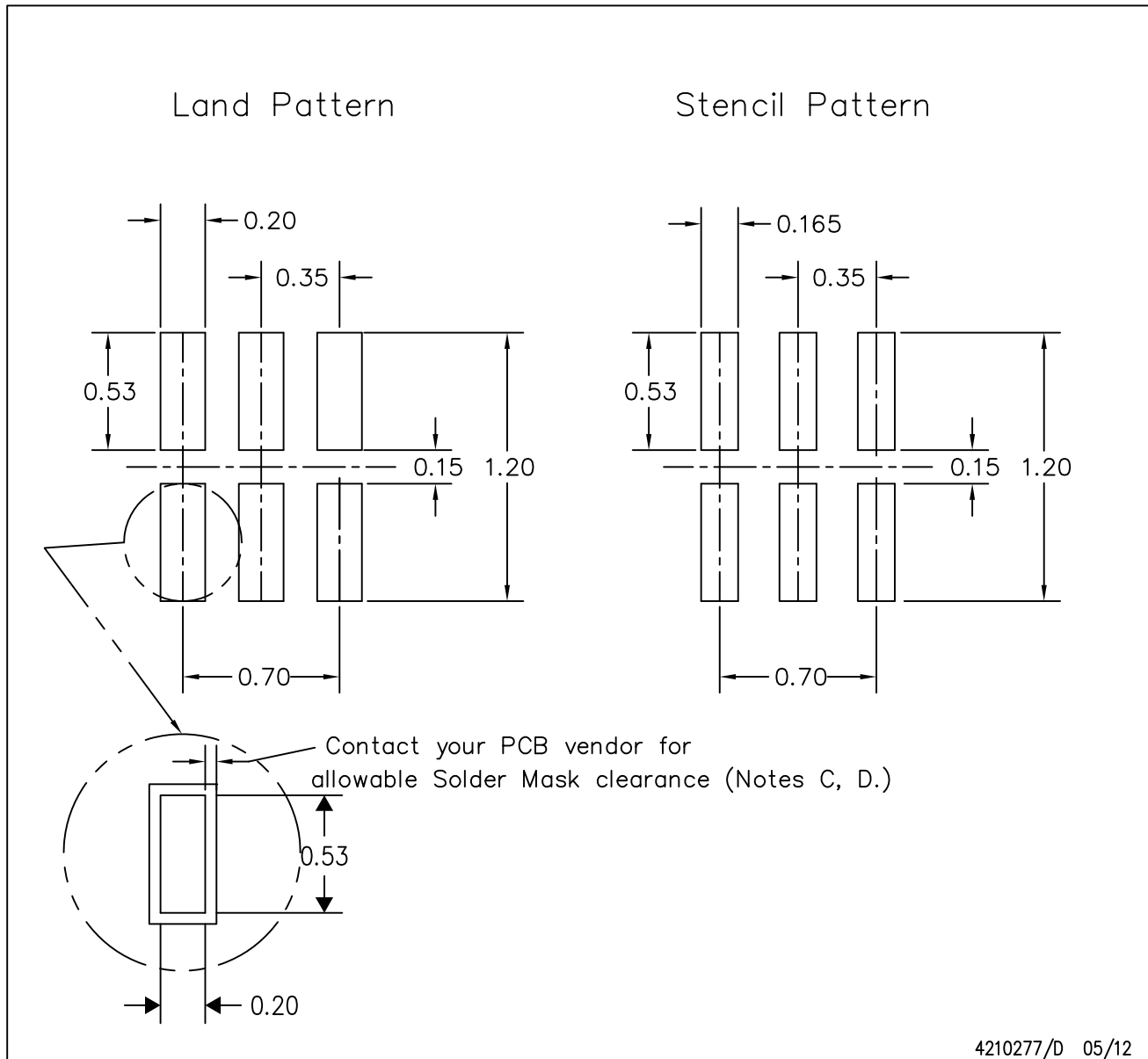


4208186/E 03/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - SON (Small Outline No-Lead) package configuration.
  - This package complies to JEDEC MO-287 variation X2AAF.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4210277/D 05/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
  - Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - Component placement force should be minimized to prevent excessive paste block deformation.

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